We claim:

1. A data slicer comprising:
a first comparator circuit that establishes a first threshold;
a second comparator circuit that establishes a second threshold; and
a third comparator circuit that establishes a third threshold;
wherein the second threshold is greater than the first threshold and less than the third threshold,
wherein each of the comparator circuits has an offset, and
wherein the first and third comparator circuits have symmetrical offsets.

2. The data slicer of claim 1 wherein the first and third comparator circuits have output circuits providing the symmetrical offsets.

3. The data slicer of claim 1 wherein each of the first and third comparator circuits includes a load resistor having a center tap and wherein the load resistor center tap of the first comparator circuit is coupled to the load resistor center tap of the third comparator circuit to provide the first and second comparator circuits with symmetrical offsets.

4. The data slicer of claim 1 wherein the first and third thresholds are equally spaced from the second threshold.

5. The data slicer of claim 1 wherein the comparator circuits are formed from complimentary metal oxide semiconductor devices.

6. A data slicer comprising:
a first comparator circuit that establishes a first threshold;
a second comparator circuit that establishes a second threshold; and
a third comparator circuit that establishes a third threshold;
wherein the second threshold is greater than the first threshold and less than the third threshold,
wherein each of the comparator circuits has an offset, and
wherein the first and third comparator circuits have output circuits providing symmetrical offsets.

7. The data slicer of claim 6 wherein the output circuit of each of the first and third comparator circuits includes a load resistor having a center tap and wherein the load resistor center tap of the first comparator circuit is coupled to the load resistor center tap of the third comparator circuit to provide the first and second comparator circuits with the symmetrical offsets.

8. The data slicer of claim 6 wherein the first and third thresholds are equally spaced from the second threshold.

9. The data slicer of claim 6 wherein the comparator circuits are formed from complimentary metal oxide semiconductor devices.

10. A data slicer comprising:

a first comparator circuit that establishes a first threshold;

a second comparator circuit that establishes a second threshold; and

a third comparator circuit that establishes a third threshold,

wherein the second threshold is greater than the first threshold and less than the third threshold,

wherein the first and third comparator circuits each includes a load resistor having a center tap, and

wherein the load resistor center tap of the first comparator circuit is coupled to the load resistor center tap of the third comparator circuit.

11. The data slicer of claim 10 wherein the first and third thresholds are equally spaced from the second threshold.

12. The data slicer of claim 10 wherein the comparator circuits are formed from complimentary metal oxide semiconductor devices.

13. An integrated circuit comprising:

a substrate of semiconductor material; and

a data slicer formed in the semiconductor material, the data slicer including,

a first comparator circuit that establishes a first threshold,

a second comparator circuit that establishes a second threshold, and

a third comparator circuit that establishes a third threshold,

wherein the second threshold is greater than the first threshold and less than the third threshold,

wherein each of the comparator circuits has an offset, and

wherein the first and third comparator circuits have symmetrical offsets.

14. The integrated circuit of claim 13 wherein the first and third comparator circuits have output circuits providing the symmetrical offsets.

15. The integrated circuit of claim 13 wherein each of the first and third comparator circuits includes a load resistor having a center tap and wherein the load resistor center tap of the first comparator circuit is coupled to the load resistor center tap of the third comparator circuit to provide the first and second comparator circuits with symmetrical offsets.

16. The integrated circuit of claim 13 wherein the first and third thresholds of the data slicer are equally spaced from the second threshold.

17. The integrated circuit of claim 13 wherein the comparator circuits are formed from complimentary metal oxide semiconductor devices.